

# Key Reconciliation Protocols for Error Correction of Silicon PUF Responses

Brice Colombier<sup>1</sup>, Lilian Bossuet<sup>2</sup>, David Hély<sup>3</sup>

<sup>1</sup>CEA-Tech DPACA, Gardanne — France

<sup>2</sup>Laboratoire Hubert Curien, Saint-Étienne — France

<sup>3</sup>LCIS, Grenoble Institute of Technology, Valence — France

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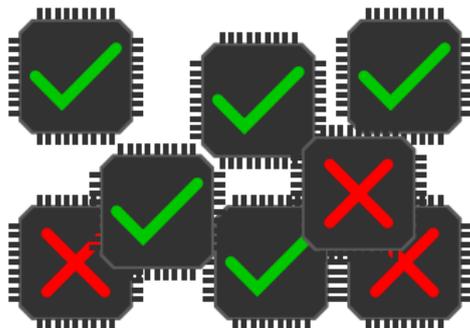
## IoT devices

- › Mutual identification
- › Authentication



## IP protection

- › ICs identification
- › IP cores identification



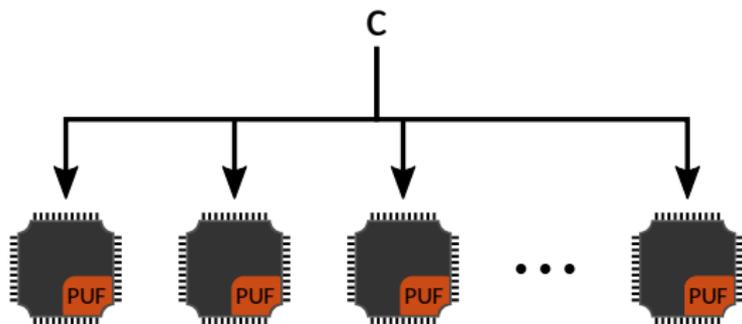
**Need for a hardware identifier as root of trust**

- 1 Physical Unclonable Functions
- 2 The CASCADE key reconciliation protocol
- 3 Attacks and countermeasures
- 4 Experimental results
- 5 Hardware implementation
- 6 Conclusion

# Physical Unclonable Functions

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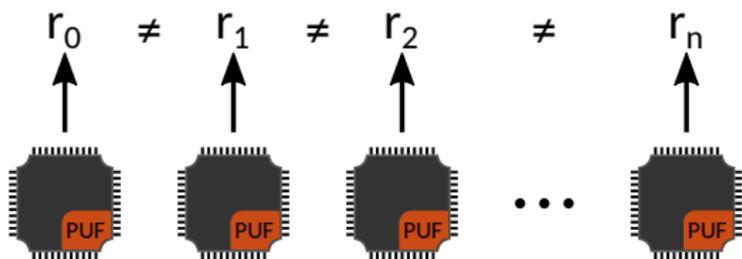


## Principle:

Extract entropy from  
**process variations.**

## Aim:

Provide a unique,  
per-device ID, thanks  
to the **inter-device**  
uniqueness.



**Different** responses to the **same** challenge.

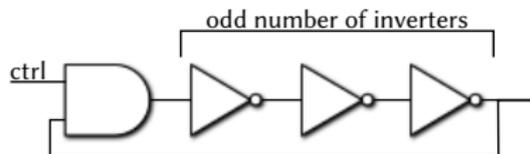
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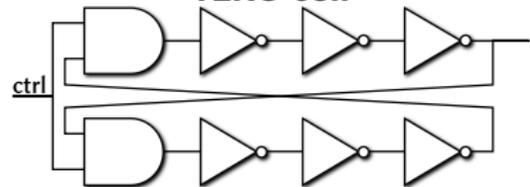
## Aim:

Provide a unique, per-device ID, thanks to the **inter-device** uniqueness.

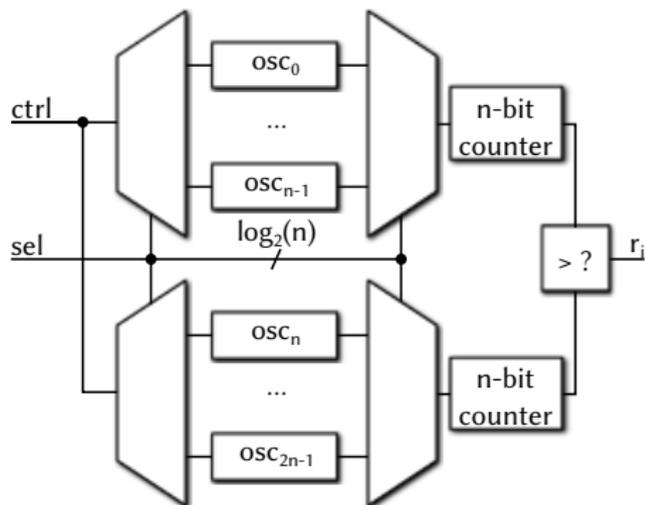
## RO cell



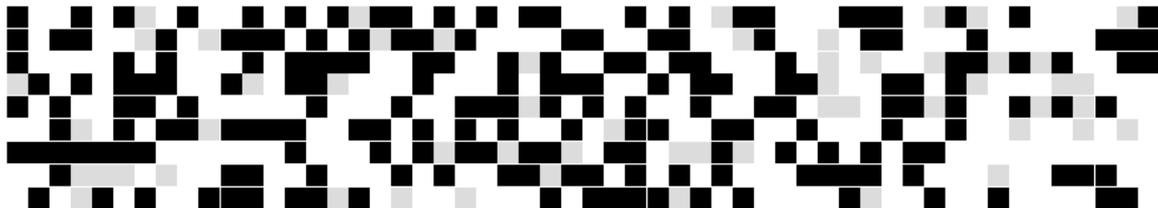
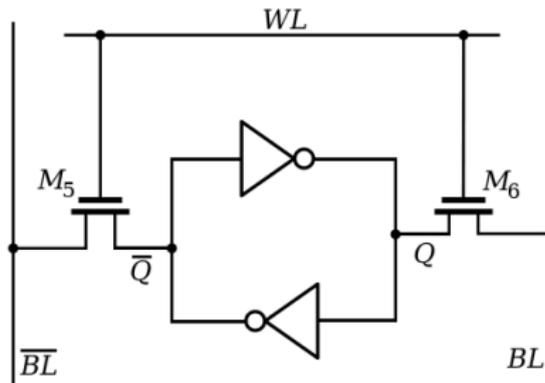
## TERO cell



## PUF architecture



## SRAM PUF



## Problem:

PUF responses to the **same** challenge **change** over time.

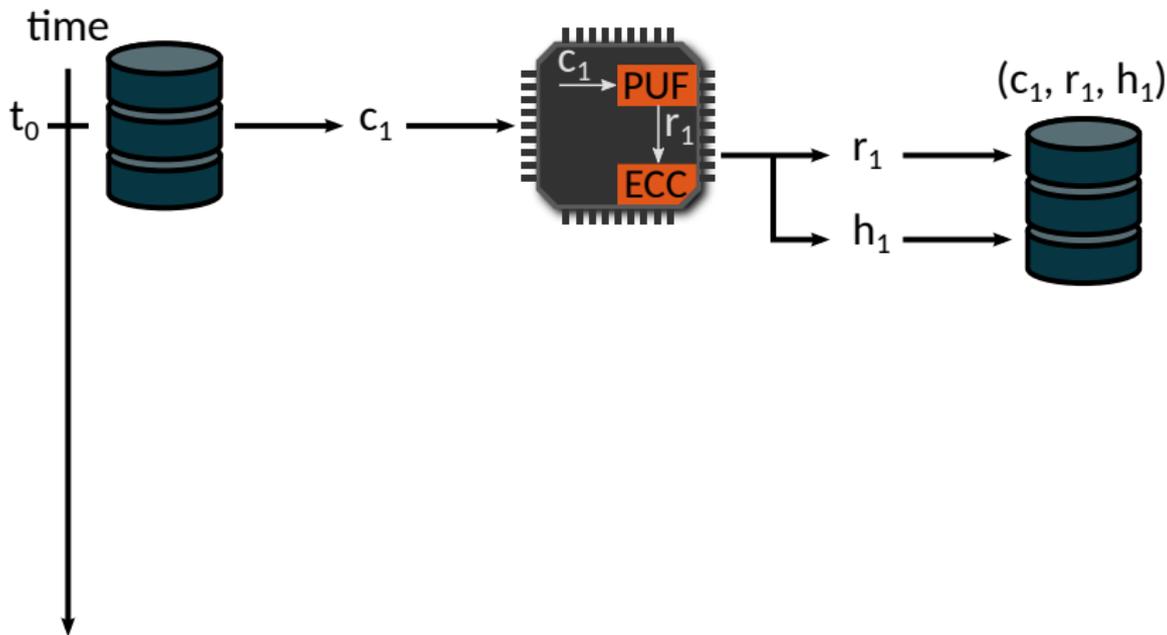
This variation depends on multiple parameters:

- PUF architecture,
- Process node,
- Aging,
- Temperature,
- Environment...

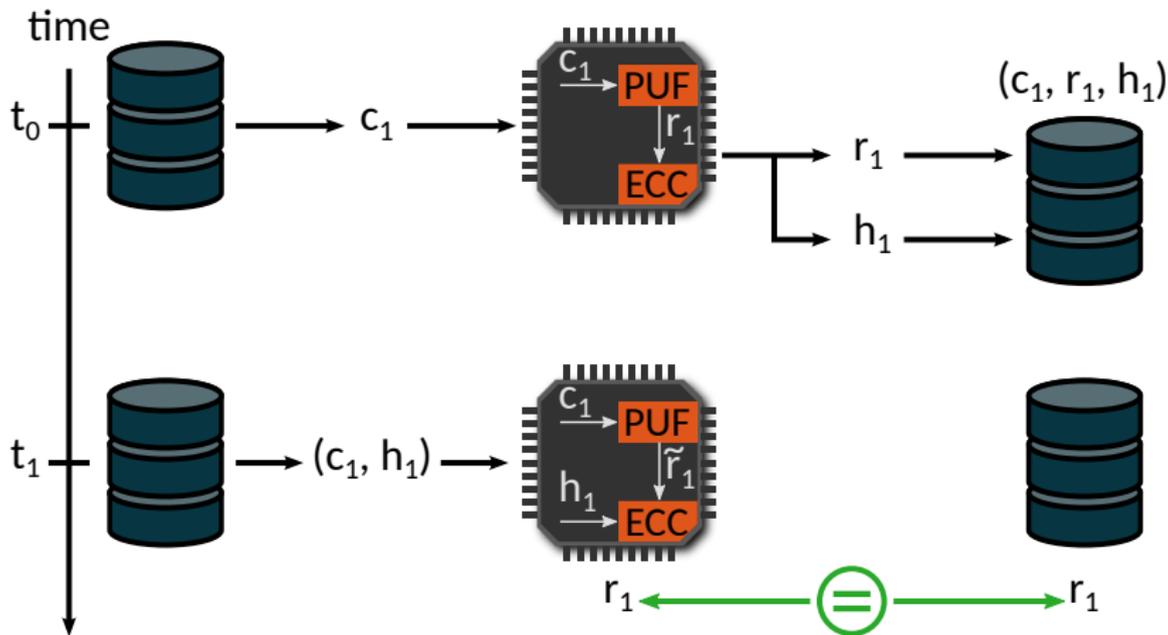
➔ The PUF response cannot be used as a **reliable identifier**.

## Solution

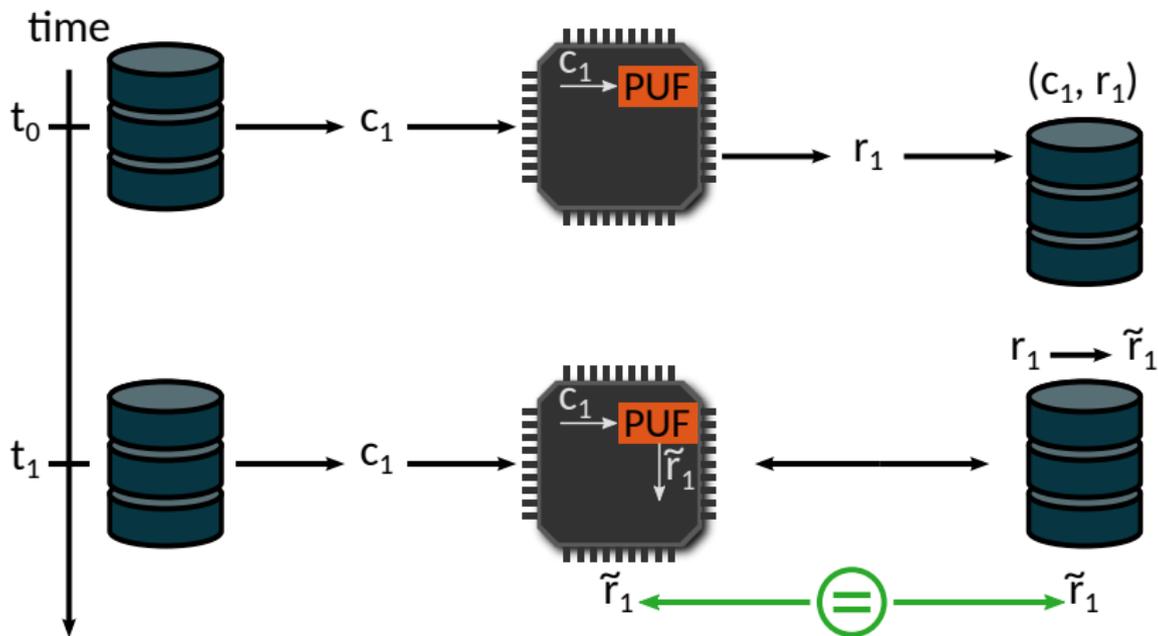
Apply a technique of **error correction** to the PUF response



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Apply a technique of **error correction** to the PUF response

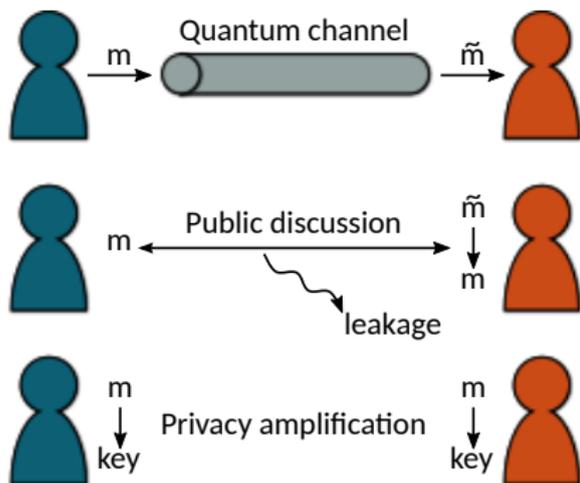
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# The CASCADE key reconciliation protocol

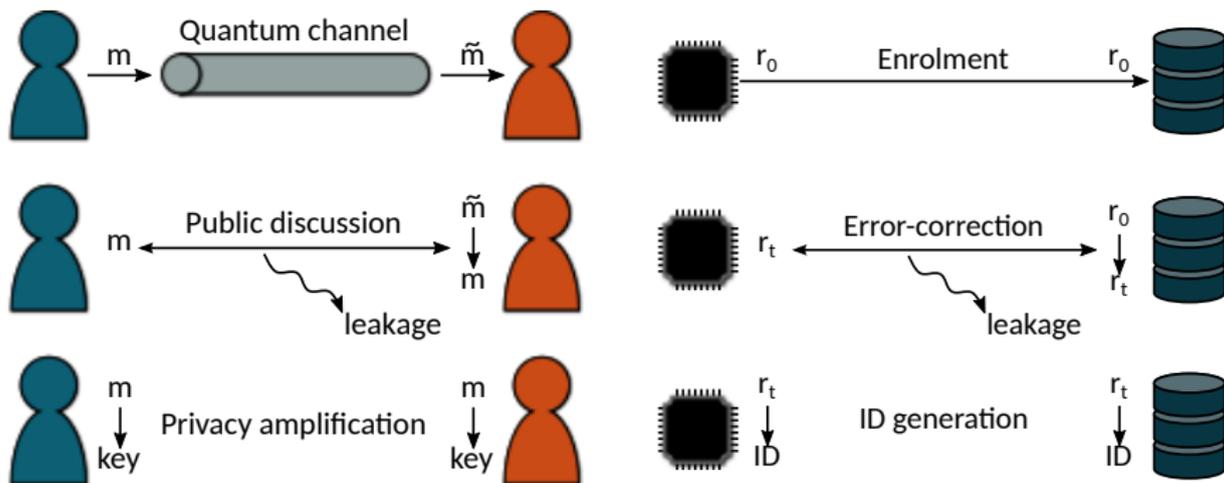
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CASCADE introduced in 1993 by Brassard and Salvail [1]



[1] Gilles Brassard and Louis Salvail. "Secret-Key Reconciliation by Public Discussion". *EUROCRYPT*. 1993, pp. 410–423.

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This could be used to derive keys from slightly different PUF responses.

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### One pass

- Perform **parity checks** on **blocks** of the PUF response,
- **Isolate** the errors using **binary search** and correct them,
- Check **current** parity of blocks and **backtrack**,
- **Increase** the block size and **shuffle** the response **randomly**.

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### Parameters

- Initial block size,
- Block size multiplier.
- Number of passes,

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### Parameters

- Initial block size,
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- Number of passes,

### Information leakage associated with the public discussion

For an  $n$ -bit response split into  $k$ -bit blocks:

- Parity checks:  $n/k$ -bit leakage.
- Binary search:  $\log_2(k)$ -bit leakage.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
---	---	---	---	---	---	---	---	---	---	----	----	----	----	----	----

Blocks of even relative parity:

$\emptyset$

Blocks of odd relative parity:

$\emptyset$

$$\text{Relative parity: } P_r(B_0, B_t) = \underbrace{\left( \bigoplus_{i=0}^{m-1} r_0[B_0[i]] \right)}_{\text{Parity of } B_0} \oplus \underbrace{\left( \bigoplus_{i=0}^{m-1} r_t[B_t[i]] \right)}_{\text{Parity of } B_t}$$

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Shuffling

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12	14	4	7	9	0	13	5	2	10	8	11	3	15	6	1
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Blocks of even relative parity:

0	1	2	3	4	5	6	7
---	---	---	---	---	---	---	---

8	9	10	11
---	---	----	----

2	10	8	11	3	15	6	1
---	----	---	----	---	----	---	---

Blocks of odd relative parity:

12	13	14	15
----	----	----	----

12	14	4	7	9	0	13	5
----	----	---	---	---	---	----	---

$$\text{Relative parity: } P_r(B_0, B_t) = \underbrace{\left( \bigoplus_{i=0}^{m-1} r_0[B_0[i]] \right)}_{\text{Parity of } B_0} \oplus \underbrace{\left( \bigoplus_{i=0}^{m-1} r_t[B_t[i]] \right)}_{\text{Parity of } B_t}$$

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
---	---	---	---	---	---	---	---	---	---	----	----	----	----	----	----

Correction

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
---	---	---	---	---	---	---	---	---	---	----	----	----	----	----	----

Shuffling

12	14	4	7	9	0	13	5	2	10	8	11	3	15	6	1
----	----	---	---	---	---	----	---	---	----	---	----	---	----	---	---

Correction

12	14	4	7	9	0	13	5	2	10	8	11	3	15	6	1
----	----	---	---	---	---	----	---	---	----	---	----	---	----	---	---

Extra correction

12	14	4	7	9	0	13	5	2	10	8	11	3	15	6	1
----	----	---	---	---	---	----	---	---	----	---	----	---	----	---	---

Extra correction

12	14	4	7	9	0	13	5	2	10	8	11	3	15	6	1
----	----	---	---	---	---	----	---	---	----	---	----	---	----	---	---

Blocks of even relative parity:

0	1	2	3	4	5	6	7
---	---	---	---	---	---	---	---

8	9	10	11	12	13	14	15
---	---	----	----	----	----	----	----

2	10	8	11	3	15	6	1
---	----	---	----	---	----	---	---

12	14	4	7	9	0	13	5
----	----	---	---	---	---	----	---

Blocks of odd relative parity:

∅

$$\text{Relative parity: } P_r(B_0, B_t) = \underbrace{\left( \bigoplus_{i=0}^{m-1} r_0[B_0[i]] \right)}_{\text{Parity of } B_0} \oplus \underbrace{\left( \bigoplus_{i=0}^{m-1} r_t[B_t[i]] \right)}_{\text{Parity of } B_t}$$

Two ways of leaking information:

- Relative parity computations,
  - 1 bit.
- CONFIRM executions on an  $n$ -bit block.
  - $\log_2(n)$  bits.

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### Example:

**128-bit** response,  $\varepsilon = 0.05 \rightarrow 7$  errors.

- 1<sup>st</sup> pass: **8-bit blocks**, **4 errors corrected**.
- 2<sup>nd</sup> pass: **16-bit blocks**, **3 errors corrected**.

Leakage:  $\frac{128}{8} + 4 \times \log_2(8) + \frac{128}{16} + 3 \times \log_2(16) = 48$  bits.

The final effective length of the response is  $128 - 48 = \mathbf{80}$  bits.

What is the lower bound on the information leakage?

It is related to the conditional entropy [2]  $H(r_t|r_0) = nh(\varepsilon)$  where  $\varepsilon$  is the error rate and  $n$  is the response length.

$$h(\varepsilon) = -\varepsilon.\log_2(\varepsilon) - (1 - \varepsilon).\log_2(1 - \varepsilon)$$

The best length we can expect for the final response is then:

$$n - nh(\varepsilon) = n(1 - h(\varepsilon))$$

### Examples:

With a 128-bit response and a 5% error rate: 91 bits.

With a 128-bit response and a 10% error rate: 67 bits.

---

[2] Jesus Martinez-Mateo et al. "Demystifying the Information Reconciliation Protocol CASCADE". . *Quantum Information & Computation* 15.5&6 (2015), pp. 453-477.

How to set the CASCADE parameters?

- **Initial block size:** depends on the error rate.
- **Number of passes:** depends on the required correction success rate.
- **Block size multiplier:**  $\times 2/\times 4$  at each pass.

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## Problem

The block size **cannot** exceed  $n/2$ .  
The **failure rate** remains **too high**.

How to set the CASCADE parameters?

- **Initial block size:** depends on the error rate.
- **Number of passes:** depends on the required correction success rate.
- **Block size multiplier:** x2/x4 at each pass.

## Problem

The block size **cannot** exceed  $n/2$ .  
The **failure rate** remains **too high**.

## Solution

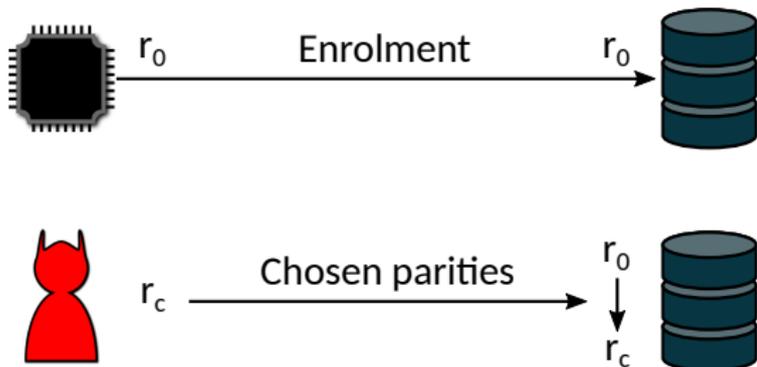
Add extra passes **without increasing** the block size.

# Attacks and countermeasures

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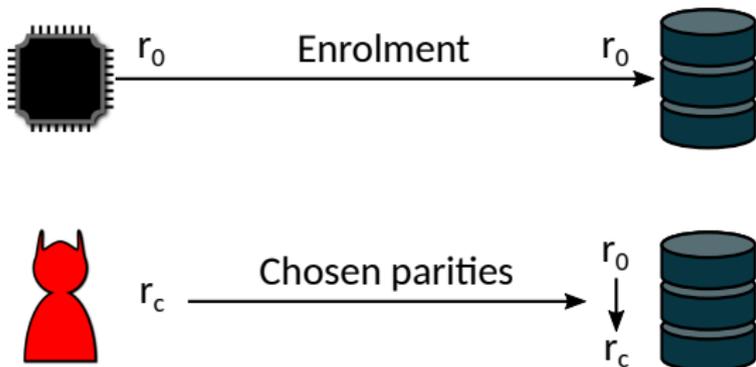
**Threat: chosen parities scenario**

An attacker wants to set a chosen response value on the server side by sending chosen parities.



**Threat: chosen parities scenario**

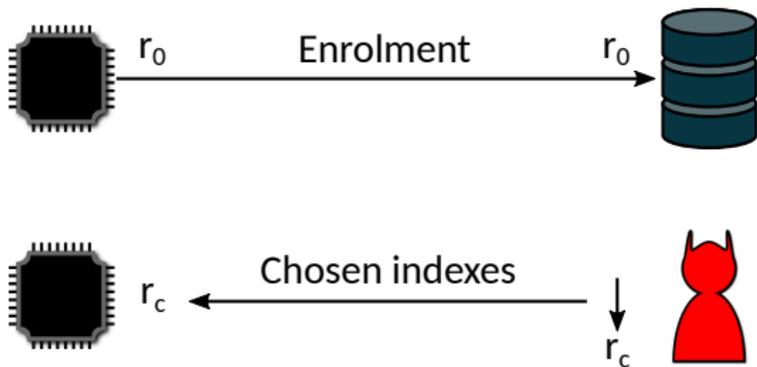
An attacker wants to set a chosen response value on the server side by sending chosen parities.

**Countermeasure:**

Limit the number of modifiable bits on the server side.

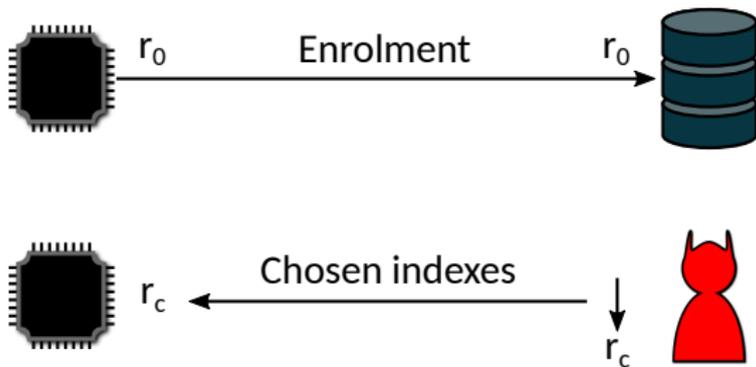
**Threat: chosen indexes scenario**

An attacker wants to **recover the PUF response** by building a sufficiently determined system of equations.



**Threat: chosen indexes scenario**

An attacker wants to **recover the PUF response** by building a sufficiently determined system of equations.

**Countermeasures:**

- ▶ Limit the number of parity values that can be sent out.
- ▶ Regenerate a new response at every protocol execution.

# Experimental results

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Several realistic PUF references:

- RO PUF in FPGA  $\varepsilon = 0.9\%$  [3].
- TERO PUF in FPGA  $\varepsilon = 1.8\%$  [4].
- SRAM PUF in ASIC  $\varepsilon = 5.5\%$  [5].

Keep **128 bits secret** from a 256-bit response with **failure rate  $< 10^{-6}$** .

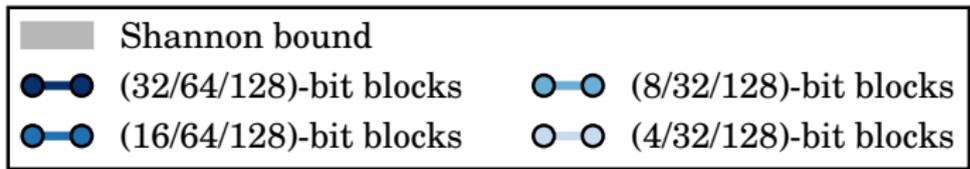
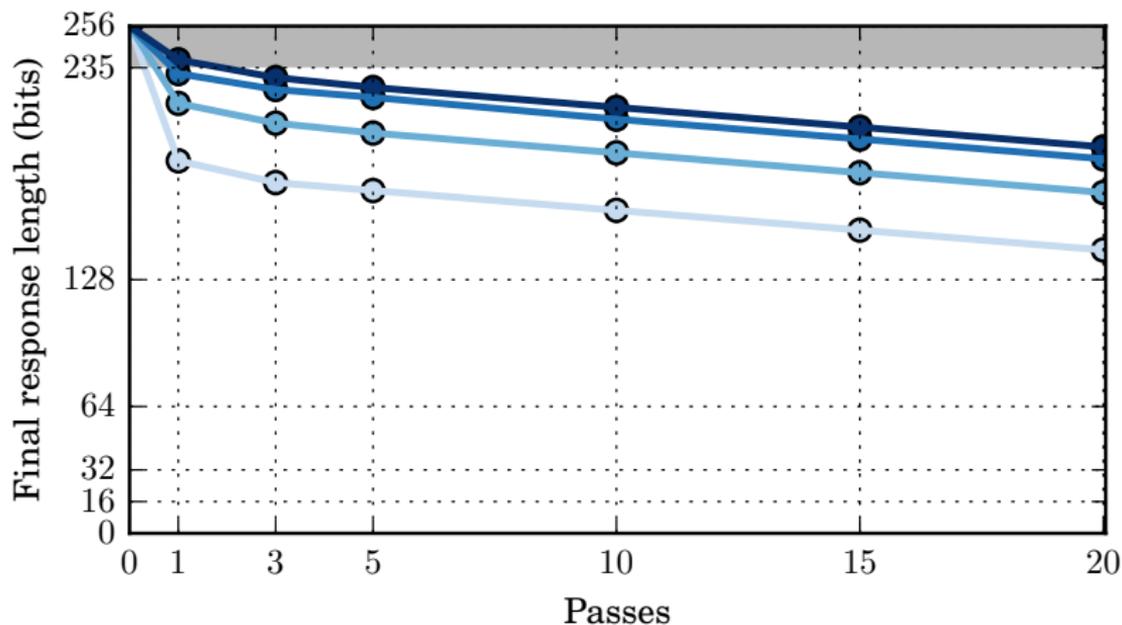
Simulation carried out on 2 500 000 responses.

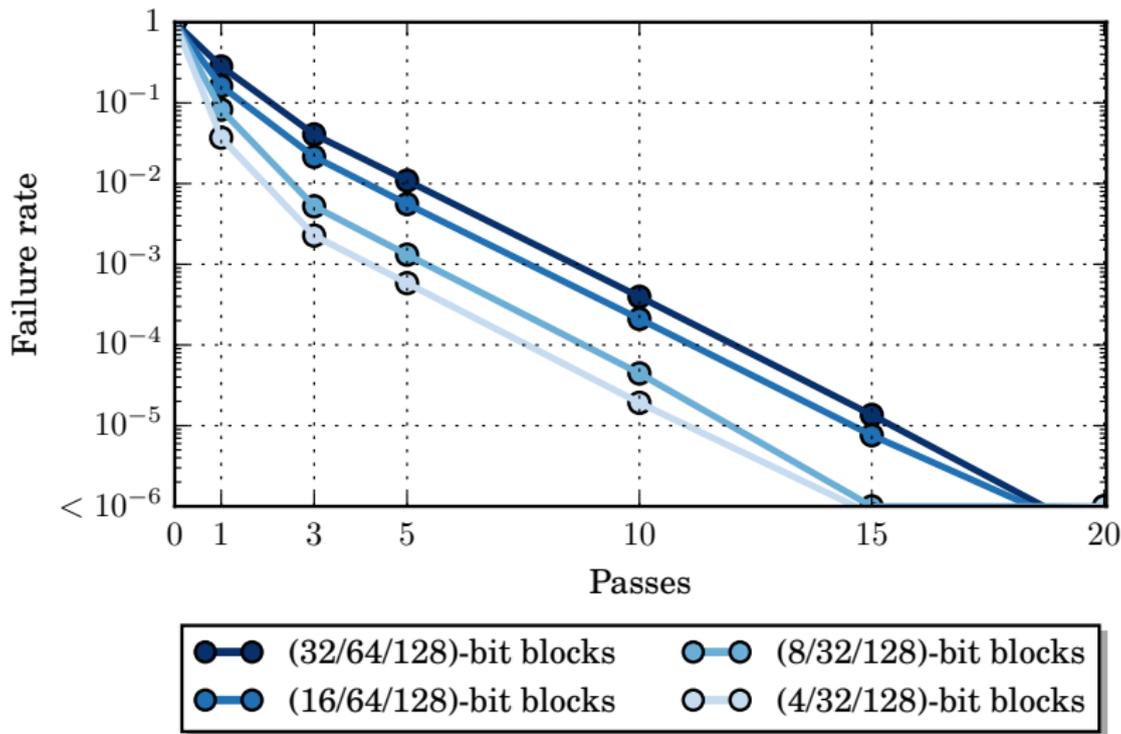
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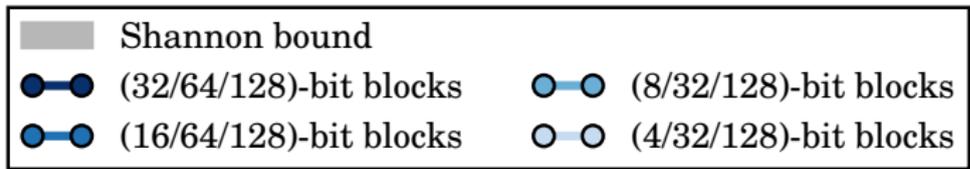
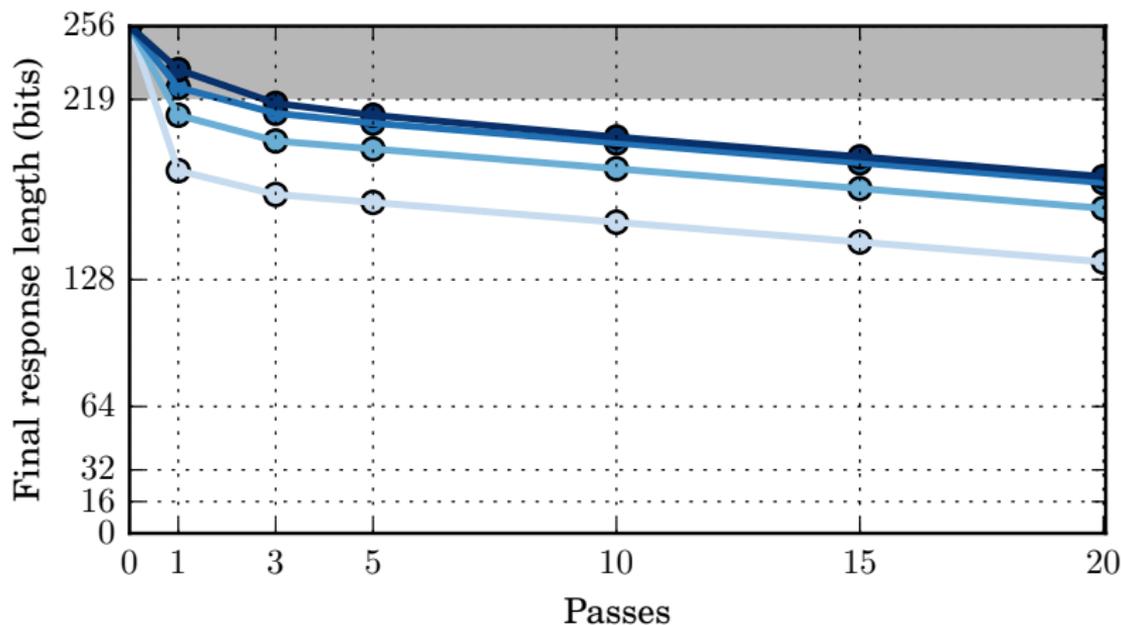
[3] Abhranil Maiti, Jeff Casarona, Luke McHale, and Patrick Schaumont. “A large scale characterization of RO-PUF”. . *HOST*. 2010, pp. 94–99.

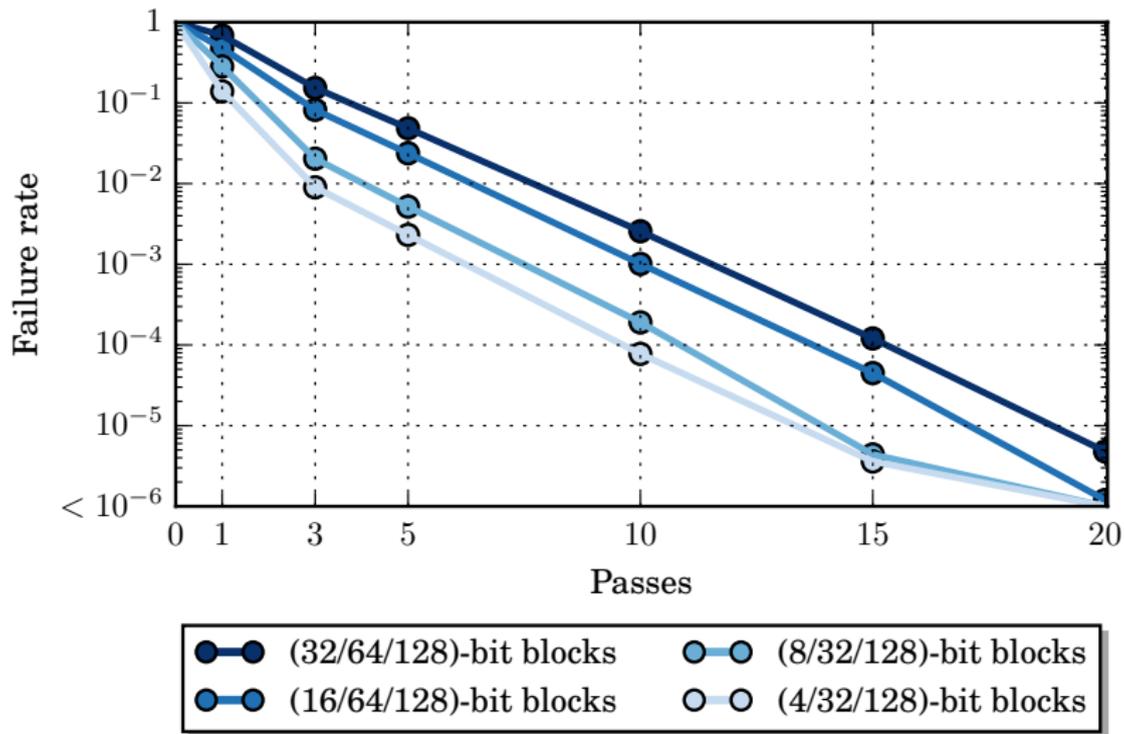
[4] Cédric Marchand, Lilian Bossuet, and Abdelkarim Cherkaoui. “Enhanced TERO-PUF Implementations and Characterization on FPGAs”. *International Symposium on FPGAs*. 2016, p. 282.

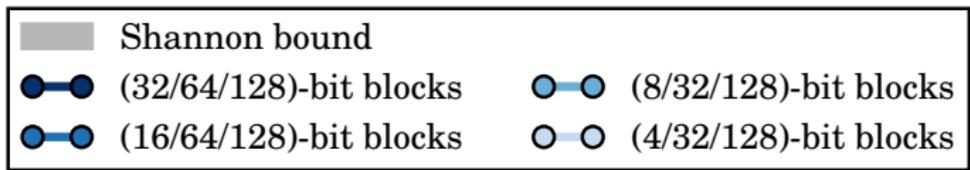
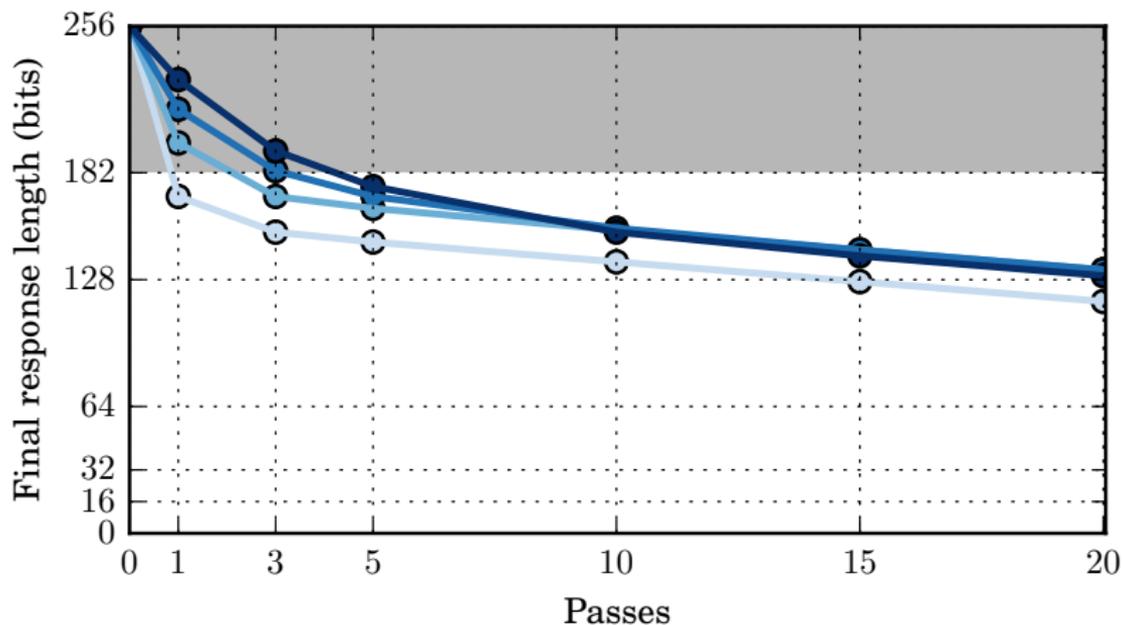
[5] Mathias Claes, Vincent van der Leest, and An Braeken. “Comparison of SRAM and FF-PUF in 65nm Technology”. *Nordic Conference on Secure IT Systems*. Vol. 7161. 2011, pp. 47–64.

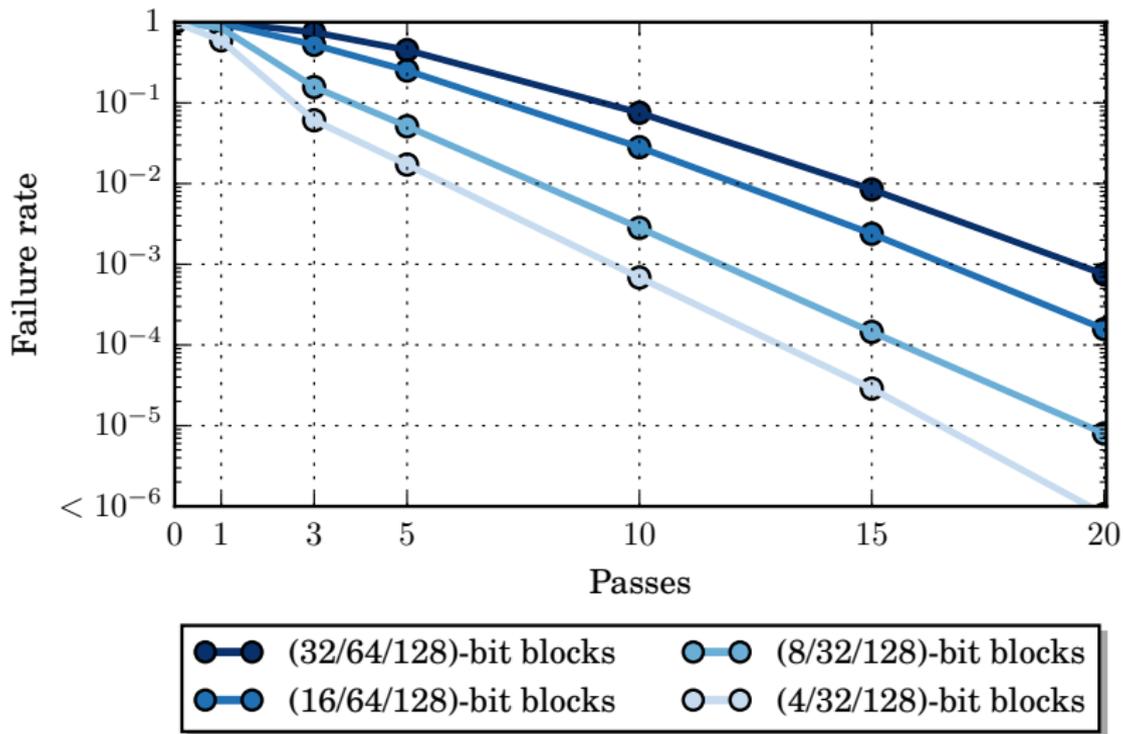






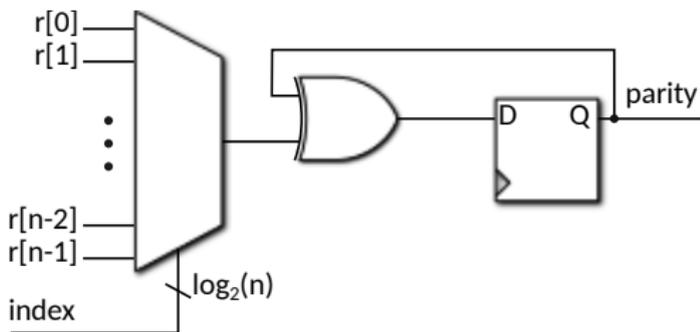




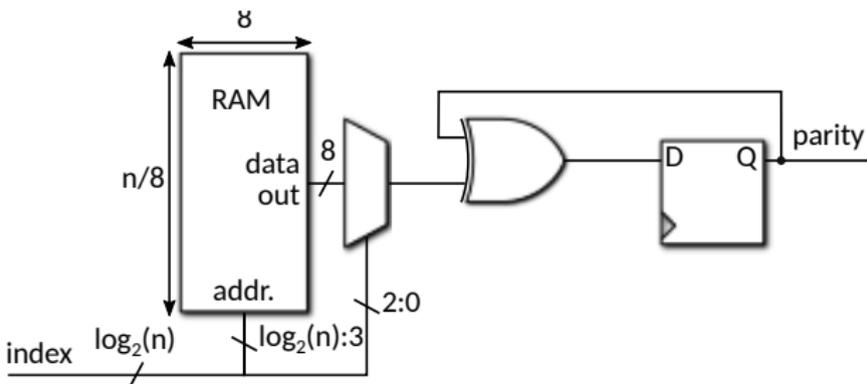


# Hardware implementation

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**Logic resources:**

- Spartan 3: 67 Slices
- Spartan 6: 19 Slices
- 0 RAM bits

**Logic resources:**

- Spartan 3: 3 Slices
- Spartan 6: 1 Slice
- 256 RAM bits

Article	Construction and code(s)	Logic resources (Slices)		Block RAM bits
		Spartan 3	Spartan 6	
[6]	Reed-Muller (4, 7)		179	0
[7]	Reed-Muller (2, 6)	164		192
[8]	Concatenated: Repetition and Reed Muller	168		0
[9]	Differential Sequence Coding and Viterbi	75	27	10752
This work: CASCADE protocol	logic only	67	19	0
	with RAM	3	1	256

[6] Matthias Hiller et al. "Low-Area Reed Decoding in a Generalized Concatenated Code Construction for PUFs". *ISVLSI*. 2015, pp. 143-148

[7] Roel Maes, Pim Tuyls, and Ingrid Verbauwhede. "Low-Overhead Implementation of a Soft Decision Helper Data Algorithm for SRAM PUFs". *CHES*. 2009, pp. 332-347

[8] Christoph Bösch et al. "Efficient Helper Data Key Extractor on FPGAs". *CHES*. 2008, pp. 181-197

[9] Matthias Hiller, Meng-Day Yu, and Georg Sigl. "Cherry-Picking Reliable PUF Bits With Differential Sequence Coding". *IEEE Trans. Information Forensics and Security* 11.9 (2016), pp. 2065-2076

# Conclusion

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Compared to existing methods:

- ✓ **most lightweight** error-correction solution of state-of-the-art,
- ✓ can reach **very low** failure rates (down to  $10^{-8}$ ),
- ✓ leakage is **limited** and **easy** to estimate,
- ✓ **parameterizable** and can be changed **on the fly**.

All code available on Gitlab:

<https://gitlab.univ-st-etienne.fr/b.colombier/cascade>

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— Questions? —