

Key reconciliation protocol application to error correction in silicon PUF responses

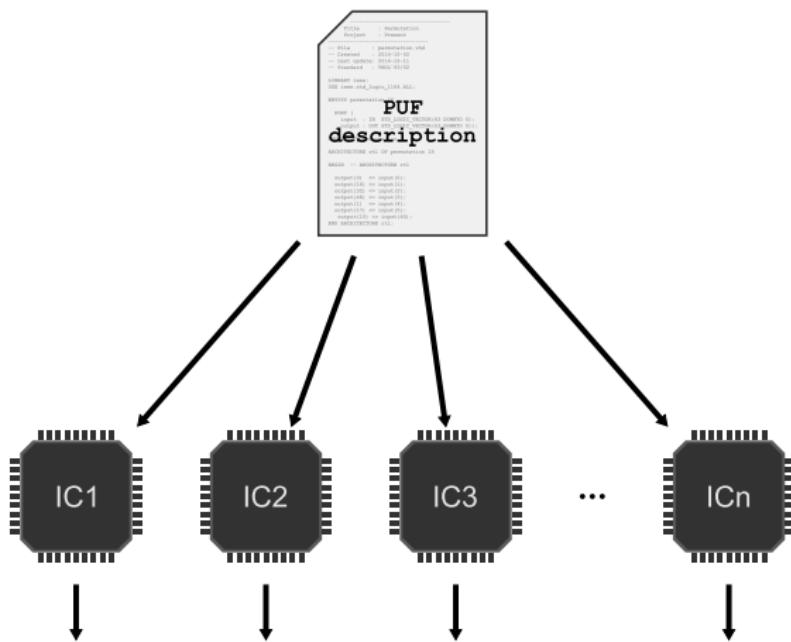
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PUFs as identifiers



Principle:

Extract entropy
from process
variations.

Aim:

Provide a unique,
per-device ID,
thanks to the
inter-device
uniqueness.

Different responses to the **same** challenge.

The instability problem



Problem:



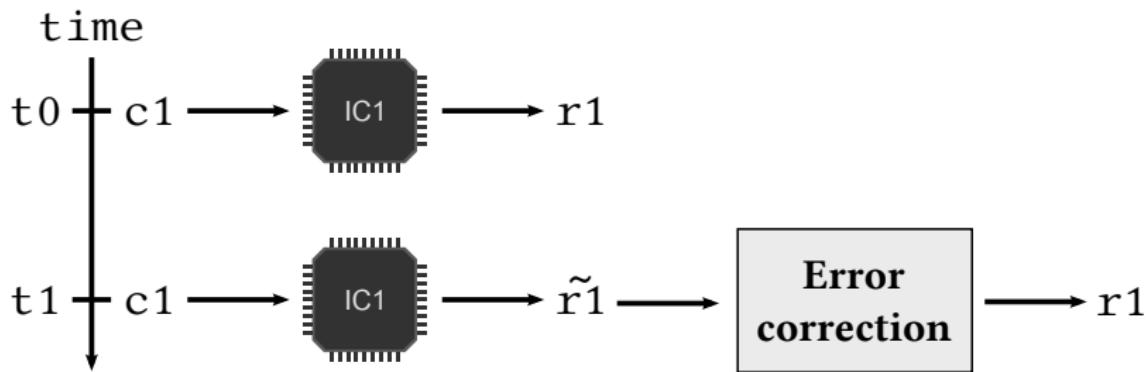
The PUF responses
to the **same** challenge
change over time.

This variation depends on multiple parameters:

- PUF architecture,
- Process node,
- Aging,
- Temperature,
- Environment...

Assumptions and requirements

Solution: Correct the PUF response.

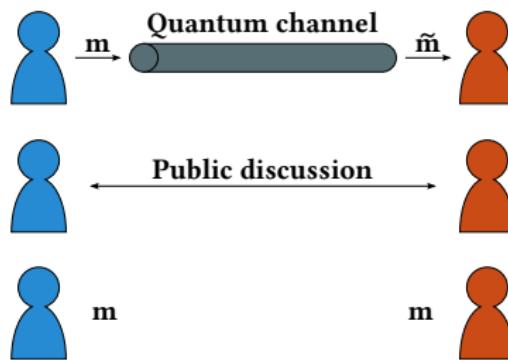


Requirements for the error correction module:

- Low area,
- High correction probability,
- Limited leakage.

Information reconciliation protocols

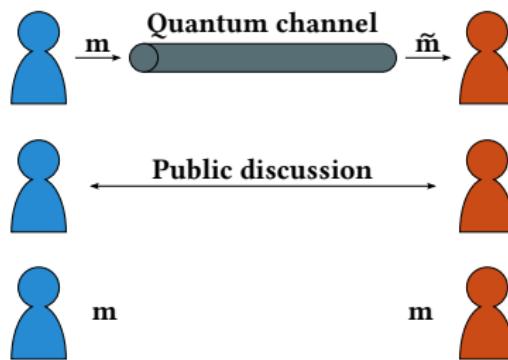
CASCADE introduced in 1993 by Brassard and Salvail¹.



¹G. Brassard and L. Salvail, *Secret-Key Reconciliation by Public Discussion*, **EUROCRYPT**, 1993.

Information reconciliation protocols

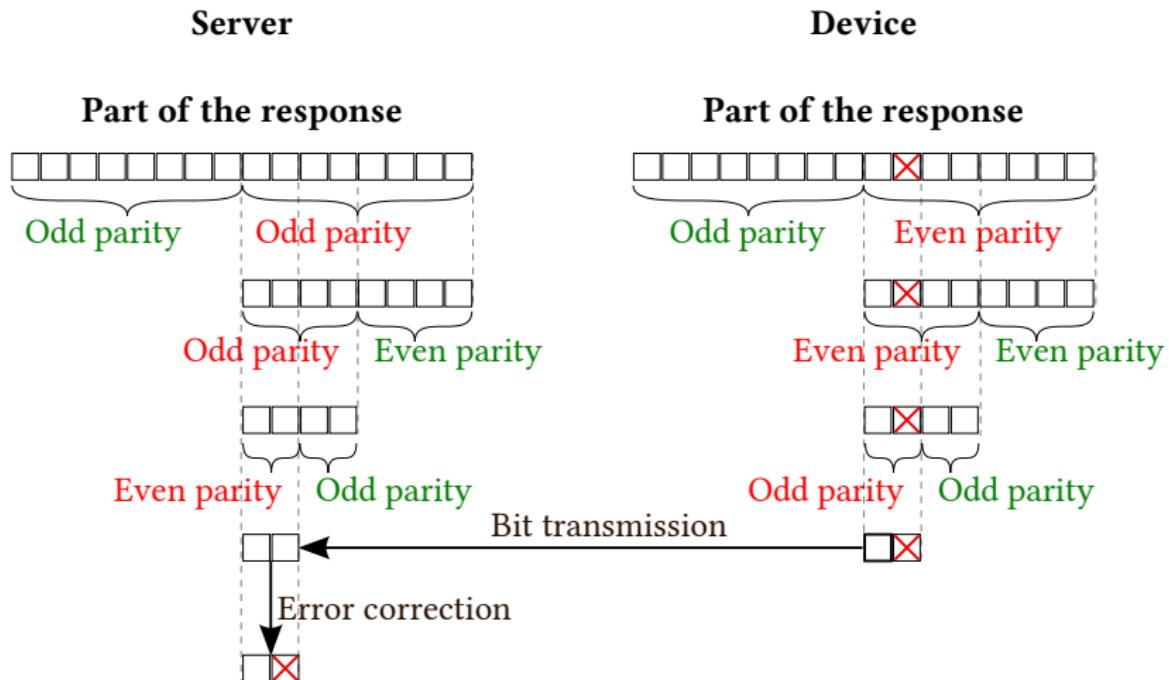
CASCADE introduced in 1993 by Brassard and Salvail¹.



This could be used to correct errors
in slightly different PUF responses

¹G. Brassard and L. Salvail, *Secret-Key Reconciliation by Public Discussion*, **EUROCRYPT**, 1993.

CONFIRM: dichotomy-based error correction



Allows to correct **one error** per pass.

Relative parity

The relative parity of two vectors V_1 and V_2 is given by:

$$P_r(V_1, V_2) = \underbrace{\left(\bigoplus_{i=1}^{|V_1|} V_1 \right)}_{\text{Parity of } V_1} \oplus \underbrace{\left(\bigoplus_{i=1}^{|V_2|} V_2 \right)}_{\text{Parity of } V_2}$$

If they are **identical** or differ in an **even** number of errors:

→ their relative parity is 0.

If they differ in an **odd** number of errors:

→ their relative parity is 1.

BINAR Y: using CONFIRM to correct multiple errors

BINAR Y method:

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
---	---	---	---	---	---	---	---	---	---	----	----	----	----	----	----

Split into blocks

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
---	---	---	---	---	---	---	---	---	---	----	----	----	----	----	----

Correction

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
---	---	---	---	---	---	---	---	---	---	----	----	----	----	----	----

Scrambling and use larger blocks

2	8	9	0	1	11	13	5	4	6	15	10	3	14	7	12
---	---	---	---	---	----	----	---	---	---	----	----	---	----	---	----

Correction

2	8	9	0	1	11	13	5	4	6	15	10	3	14	7	12
---	---	---	---	---	----	----	---	---	---	----	----	---	----	---	----

} Pass 0

} Pass 1

Backtracking

After a pass, all the blocks have an **even** relative parity.

- if an error is corrected on a bit from this block in a subsequent pass, then its relative parity becomes **odd** again.
- one more error from this block can be corrected.

Required: two lists storing blocks according to their relative parity.

Correcting an error at index i makes blocks containing index i move from one list to the other (**their relative parity changed**).

Error correction is carried out until there are **no more blocks of odd parity**.

The CASCADE protocol

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
---	---	---	---	---	---	---	---	---	---	----	----	----	----	----	----

Blocks of even
relative parity:

\emptyset

Blocks of odd relative
parity:

\emptyset

The CASCADE protocol

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
---	---	---	---	---	---	---	---	---	---	----	----	----	----	----	----

Correction

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---	---	---	---	---	---	---	---	---	---	----	----	----	----	----	----

Blocks of even
relative parity:

0	1	2	3	4	5	6	7
---	---	---	---	---	---	---	---

8	9	10	11	12	13	14	15
---	---	----	----	----	----	----	----

Blocks of odd relative
parity:

∅

The CASCADE protocol

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Scrambling

12	14	4	7	9	0	13	5	2	10	8	11	3	15	6	1
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Extra correction

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Blocks of even
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relative parity:

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8	9	10	11				

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Blocks of odd relative
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Blocks of odd relative parity:

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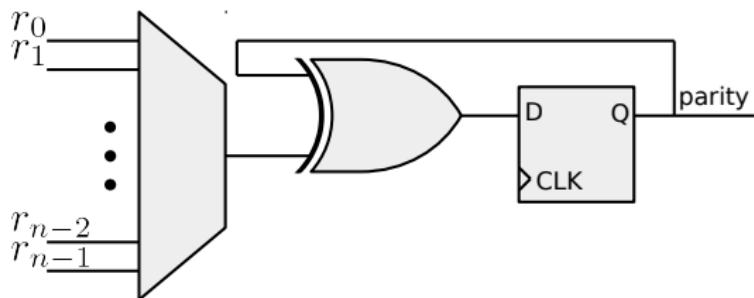
For the **same number of passes**, the CASCADE protocol allows to correct **more errors** than BINARY.

Implementation

Only **parity computations** are embedded on the device.
All other computations can be done **on the server**.

Requirements:

- A multiplexer,
- One XOR gate,
- One D flip-flop.



Example: 256-bit response

Xilinx Spartan 6: 19 Slices

State-of-the-art error correcting codes implementation:

Reed-Muller (4, 7): 179 Slices
BCH (255, 21, 55): >60 Slices

Conclusion

Compared to existing error correcting codes implementations:

- similar latency,
- can reach the same very low failure rates (10^{-6}),
- leakage is easy to estimate and control,
- at least 3x fewer on-chip logic resources.

Interesting option for error-correction of PUF responses.

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- leakage is easy to estimate and control,
- at least 3x fewer on-chip logic resources.

Interesting option for error-correction of PUF responses.

— Questions? —